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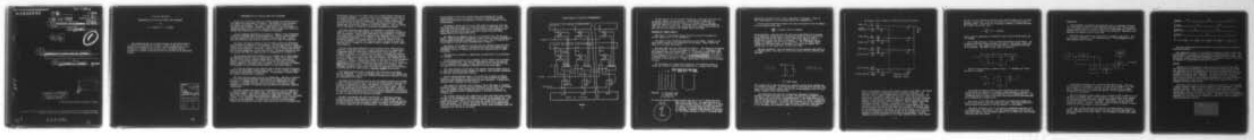

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(10) C. F. Althouse & A. J. Hopkins
author

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U. S. Navy Electronics Laboratory, San Diego 52, California

Technical Memorandum

INSTRUMENTATION FOR DIGITAL SONAR DATA PROCESSING

by

C. F. Althouse, A. J. Hopkins

(This memorandum has been prepared because the information herein is believed to be useful in this form to others in NEL and to a few persons or activities outside of NEL.) This memorandum should not be construed as a report as its only function is to present for the information of others a small portion of the work done on the associated problem.

INSTRUMENTATION FOR DIGITAL SONAR DATA PROCESSING

The Purpose of this document is to outline a broad and flexible program to mechanize and process sonar data using digital techniques. The methods will be elementary but capable of expansion. They shall be accomplished by commercially available digital computer components. There shall be the very minimum of engineering required of a specific component nature; rather, the tasks will involve the fitting together of the elements as purchased.

A very elementary application upon which to commence is the enchancement of data of a scanning sonar through integration. Various storage elements have been employed in the past to attempt to achieve this end. However, they have generally been severely restricted in the range of integration.

In effect, the data is broken up into increments which are determinable from the physical constants of the equipment. For any application of significance over a broad area, it is easy to see that the number of such increments will be in the thousands. Therefore, a device such as a cathode ray tube has been utilized extensively for such applications. The major restrictions upon its utility have been the range and rate of integration it is capable of.

The next major improvement appears to be a storage tube of which several are undergoing study or test for applicability. These will be significant, but will still lack the inherent demand that an ultimate conversion to numerics is eventually required in order to process the data by automatic digital computers. When this stage is reached, it is conceivable to commence the employment of more sophisticated methods of statistical analysis.

It is not the purpose of the proposed work to become involved in the problems of the finer grain analysis phase; rather, it is to convert to numerics and study the feasibility of going further. An assessment of results after the initial phase should be revealing.

The first task will entail the use of a CTFM sonar. The data is resolved in a set of frequency analyzers which normally are scanned and the output displayed on a cathode ray tube. There will be no modification of this operation. A separate parallel scan will be made of the analyzer filter elements and converted to a digital value and thence processed and displayed independently.

The basic element about which this instrumentation is to be centered is a commercial magnatic core memory unit. This unit has available 1092 words in a serial manner. Each word is composed of eight parallel digits. The entire unit is self-contained including power supply and is 21 x 23 x 14 inches in size. It is completely transistorized and represents a fairly "stable" point in design technology. In other words, until new film type memory elements are commercially practical, these core units will be in quantity use.

Functionally, the core unit memory would allow digital design techniques to be employed immediately. The form factor of such techniques as employed in the future may differ considerably. Size will be greatly reduced. Speed of operation may be improved considerably. However, from an engineering point of view the present speed of 20 microseconds per word cycle offers enough range to make some progress in techniques possible. Even the present size of the memory is compatible with present equipment and methods.

With this particular core memory, it is possible to integrate over a range of 0 to 256 with 1092 separate and individual integrators available in 21.84 milliseconds. This is many times faster than necessary in a scanning sonar application, so extensive computation and comparing could be achieved in a practical application. For example, if the sonar had a projector-hydrophone beamwidth of 3 degrees and if the range were broken up into 52 or less increments, a sector of 63 degrees could be covered with this unit. There would be no changes in the present analysis equipment or sonar operating parameters.

The use of the 1092 integrators on the 63 degree sector would serve as a basis for a technique trial over a large enough area to be of significance. An infinite range of "persistence" characteristics can be achieved. For example, in operation, the amplitude of the signal is sampled and converted to binary digits at each of the 52 range increments in a programmed sequence until the twenty one 3 degree beams have been scanned. This information can be stored or added to indefinitely, perhaps so long that all of the integrators become full. However, a number which can be of any value up to 256 can be subtracted from each of the integrators which would serve to give a controlled numeric decay characteristic. With some complication of equipment, each individual integrator could be made accessible for reduction in value without disturbing any of the others giving a selective erasure characteristic.

This digital approach leads to automatic detection which is extremely easy to instrument. A certain preassigned number can be set and compared with the 1092 integrators, and the most elementary warning device employed to sense the exceeding of this number.

The range of the integrators and the ease of sequencing allows much freedom so that a program centered largely upon the experimental rather than upon the theoretical approach can be taken. Furthermore, the problem of such data reduction is not without theoretical support in the field of radar. Much of this high speed data can be extrapolated in terms of slower sonar constants. This proposed instrumentation would allow the similar techniques to be applied to sonar with the same philosophy but with immensely simplified instrumentation due both to reduced speed and advanced technology.

The basic core memory unit would cost $19,000. A high-speed analogue to digital converter and arithmetic units would cost about $8,000. Thus, a minimum expenditure of $27,000 would be required to enable a starting point to be reached which would take advantage of years of research and development in the digital computer field in instrumentation. The timing is opportune, for

a point appears to have been reached where the functional use of such instrumentation will be wide spread in industrial electronics enabling future operational device development to utilize further advances in the optimum manner.

The magnetic memory unit will store 1092 words of 8 parallel bits each. This means there are 8 magnetic core matrix planes of 1092 cores each. The planes are 39 by 28 elements each. The read-in and read-out gating is all done within the unit; it is only necessary to provide load and unload signals which are 2 microsecond pulses.

The inputs to the magnetic cores are on 8 parallel wires, one for each matrix. Digitalized signal information is fed to these 8 inputs simultaneously from an analog to digital converter and 8 flip flops. This is shown on the block diagram of the auxiliary instrumentation in figure 1.

The outputs of the magnetic cores are also on 8 parallel wires and need a summing network for read-out, 8 reinsertion flip flops, and suitable gates and adding circuits to complete the unit for the proposed method of signal processing.

The additional circuitry is commerically available and will be purchased in a package.

The FM analyzer filters will be sampled, but the outputs will be treated in the following manner. The output of each channel will be rectified and fed to a capacitor, the charge on this capacitor will be read-out and then the capacitor will be discharged to prepare it for the next sample.

The characteristics of the memory unit proposed requires timing cycle of at least 20 μ seconds between loadings, or read-in, with alternate unloadings, or read-out, 10 μ seconds after read-in.

The 20 μ second analyzer sample will be fed into an analog to digital converter. This device will take the pulses from the analyzer and convert them to digital information proportional to their amplitude. A commercially available unit is planned for this function.

This output on 8 parallel wires from the 8 input flip flops is connected through 8 "adders", with the reinsert information, to the input of the storage unit. The outputs of the storage unit, also on 8 parallel wires, are connected through a suitable summing network to the read-out system, PPI, recorder, etc.

The storage outputs are also connected to 8 more flip flops whose outputs are fed into the aforementioned "adders" and thence to the storage unit. Thus a signal, if it has appeared once, will be read-out and reinserted into the memory indefinitely. All of the flip flops are cleared with a reset pulse after each sample. The "adders" add the new digital pulse information from the input flip flops to the old information, if any, from the memory output and reinserts it at the old or new levels.

BLOCK DIAGRAM OF AUXILIARY INSTRUMENTATION

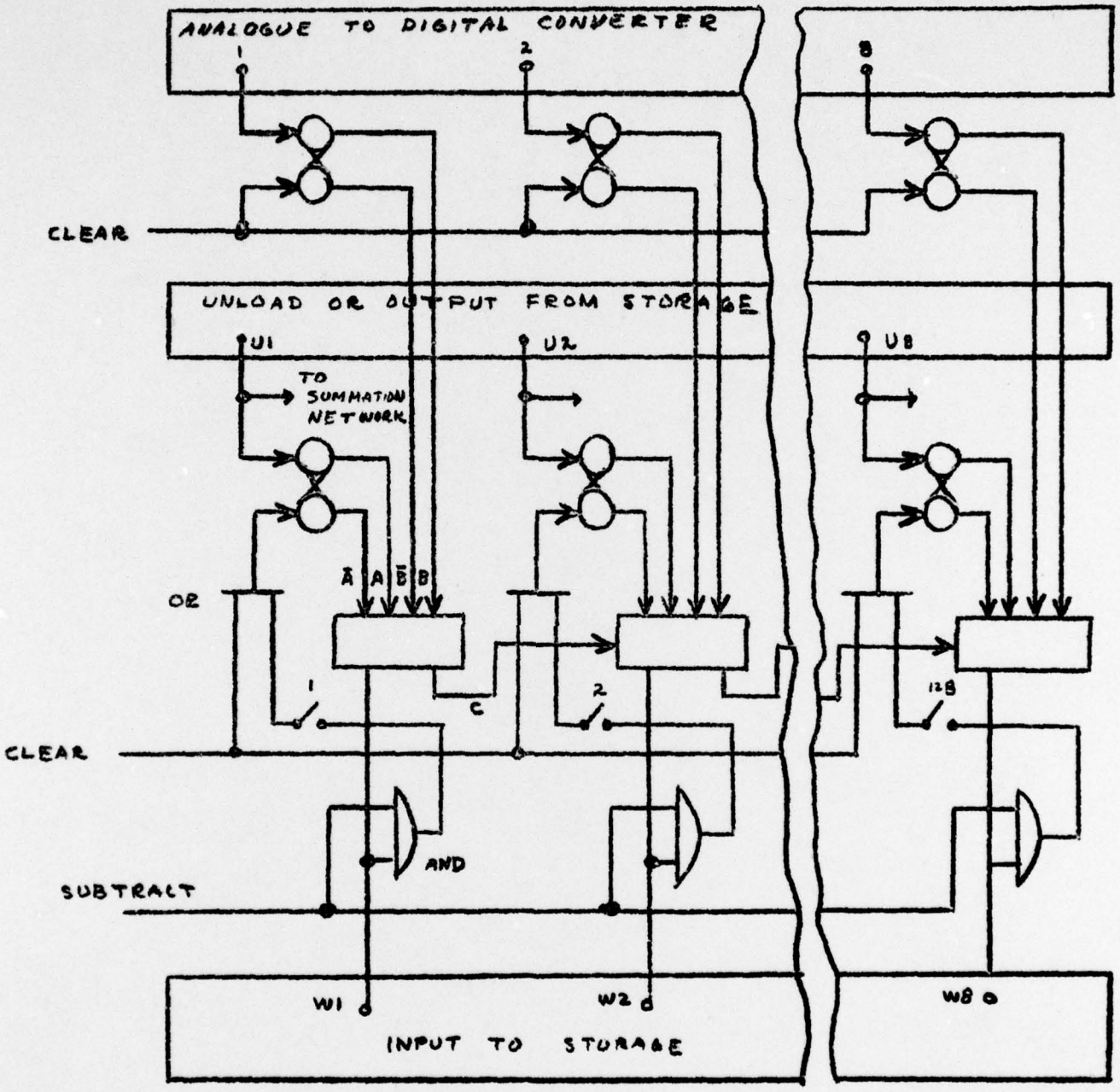


Figure 1

If this process were to continue indefinitely, the memory would soon fill up, unless cleared. To prevent this, a fixed amount of signal may be continually subtracted from the amount in the storage unit so that non-repetitive signals will die out. A subtract pulse is connected through an "and" gate with the input to the storage and then a manual switch to an "or" gate with the clear pulse to the storage output flip flops.

Operation of "Adder" Circuits

The outputs of the analog voltage to digits convertor flip flops are strictly binary "yes" or "no" information.

The output of the reinsertion flip flops is also binary. Whether or not these operate depends on the information in the memory. These outputs are added in a one digit adder matrix.

The first adder has four inputs and two outputs. The inputs are designated A and $\bar{A}$, B and $\bar{B}$, The unit is arranged so that $A \cdot \bar{B} + \bar{A} \cdot B$ produce a sum pulse which is fed to the storage unit. $A \cdot B$ produces a "carry" pulse which is connected to the next adder. This unit and the 6 following it will have 5 inputs, designated A, $\bar{A}$, B, $\bar{B}$, and C. $\bar{C}$ is generated internally. The unit is so arranged that a sum pulse is produced if the following pulses are present, $A\,\bar{B}\,\bar{C}$, $\bar{A}\,B\,\bar{C}$, $\bar{A}\,\bar{B}\,C$ and $A\,B\,C$. A carry pulse occurs if AB, BC or AC is present, (or ABC).

By this method, if a signal keeps repeating, it is gradually moved up through the register increasing the probability of it being a true target.

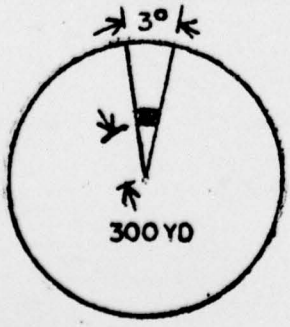
TRUTH TABLE FOR ADDER LOGIC

A	$\bar{A}$	B	$\bar{B}$	C	$\bar{C}$	SUM $(A \cdot B) \dotplus C$	C' CARRY
1	0	1	0	1	0	1	1
0	1	1	0	1	0	0	1
1	0	0	1	1	0	0	1
0	1	0	1	1	0	1	0
1	0	1	0	0	1	0	1
0	1	1	0	0	1	1	0
1	0	0	1	0	1	1	0
0	1	0	1	0	1	0	0

$0 \cdot 0 = 0$ $\quad 1 \cdot 0 = 1$ $\quad 1 \cdot 1 = 0$ $\dotplus$

NOTATION: $(\cdot)$ indicates "and"
$(\dotplus)$ indicates "or"
AB is also $A \cdot B$

The required resolution should be based upon the use of a 3 degree beam and a mean range of 300 yards. The range resolution to make an approximate square at this range is 15 yards on a side. If then 600 yards or double the mean is to represent the maximum range and 450 yards is to be displayed, a minimum of 300 channels is necessary. If a 50 channel analyzer is used, a resulting range



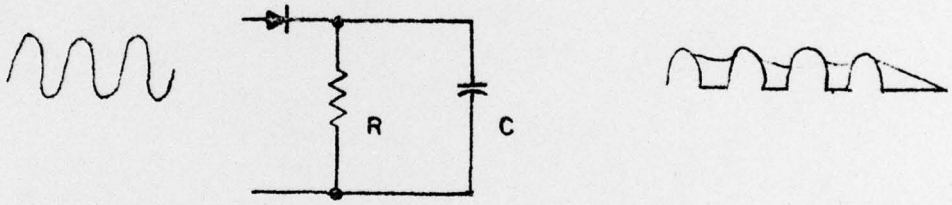
resolution of 9 yards results, with a mean range of 150 yards. Either of these values appear to be a reasonable number for consideration.

If 50 of the 52 available channels are used and allowed to fill the memory over a 63 degree sector, then

$$\frac{1092}{52} = 21 \text{ beams, each of 3 degrees}$$

can be processed. Also the scan rate of 6 rpm or 360 degrees in 10 seconds or 36 degrees per second means an integration interval of 1/12 second is the maximum tolerable at this speed, since it takes that length of time to mechanically position the beam one beamwidth. If the integration time is longer, the response will not be full amplitude. For a 50 channel system working on a 1500 cycle band, the bandpass is 30 cycles per channel for a buildup time of 1/30 second which is within the limit.

The data presented to the core memory will be 21 sequential beam widths or a 63 degree sector. The output of each filter channel will be rectified, and detected.

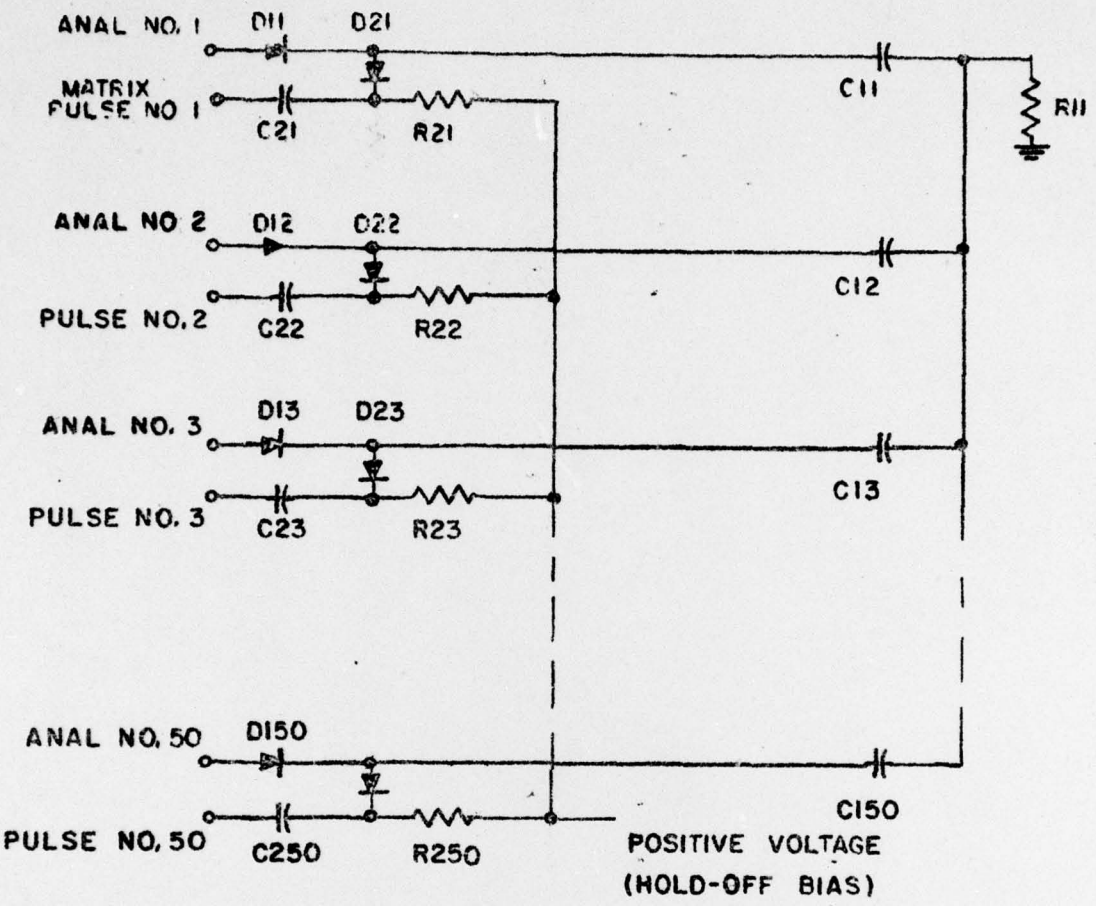


RC = 1/30 second

This output shall be made available to a sequential switch which combines the 50 individual responses. If the buildup time is 1/20 second and the decay time equal, the total filter response time is 1/15 second assuming a cycle of cycle dynamic response filter characteristic.

One fundamental variation from conventional techniques of frequency analyzers as used in FM sonar will be used. The data to be presented to the core memory will be discretely "compartmentalized". This means there will be capacitor integration but the charging capacitor will be "cleared" immediately after it has been sampled. In effect, this operation will be an integrator in the strict sense, and it is this output that gets a numerical value assigned to it. Therefore, care should be taken in the design of this component.

An example of the integrator switcher may appear as follows:



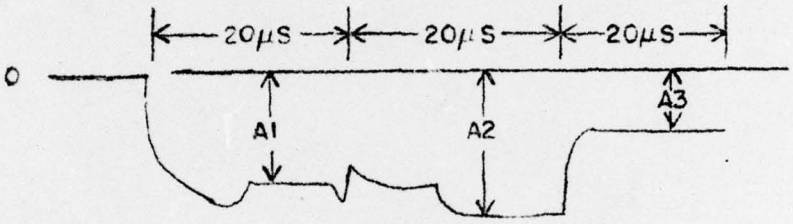
Each of the analyzer filters would provide an input to the switch. The output would be rectified and integrated by the integrating capacitors. The capacitor would be sampled sequentially by the pulses from the matrix. The diode D11 in the analyzer signal lead is merely a half wave rectifier; the other diode, capacitor, and resistor, D_{21}, C_{21}, and R_{21} serve as a clamp and sampler. A positive bias voltage exceeding the maximum integrated voltage disconnects the diodes D_{2n} from the operation. When a negative pulse from the matrix overrides the bias, a particular diode will conduct. This conduction allows the integrating capacitor to discharge through the diode and the resistors R_{2n} and R_1, the common load resistor. The voltage caused by the discharge current through R_1, is the desired signal. It is desired to keep the resistance in the total circuit as low as possible to allow the capacitor to become discharged in less than 10 microseconds. The diode resistance can be minimized by use of a high conduction diode. This implies

the use of a low impedance switching voltage from the matrix and a low value for R_{21}. A guess on R_1 would be 1000 ohms with R_{21} at 470 and almost any germanium diode. This would give a discharge resistance of about 2000 ohms. If $t = RC$ is to be 10^{-5}, then

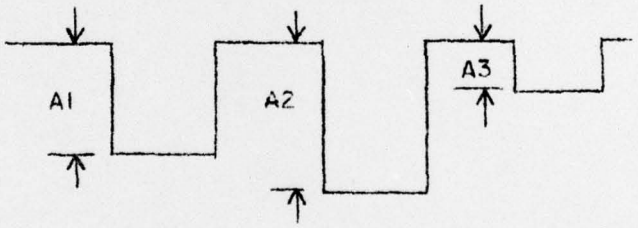
$$C = \frac{10^{-5}}{R} \quad \text{or} \quad C = 0.005\ \mu f$$

Such a value of capacitance is relatively easy to get in stable values and low leakage.

The voltage across R_1 is to be converted and applied to the memory. An analogue-to-digital voltage converter is required. The digital output must be in parallel. The conversion must take place in considerably less than 20 microseconds. The input is very likely to appear as:



About 3/4 of the period is useful or 15 μ s. A converter can "slice" the above to provide.



An analogue-to-digital converter would essentially process the above information by the operation of a digital storage register, a digital-to-voltage conversion network, a pulse comparator, and a programming unit. The programming causes a series of decisions involving successive approximations, and is actuated by a trigger pulse.

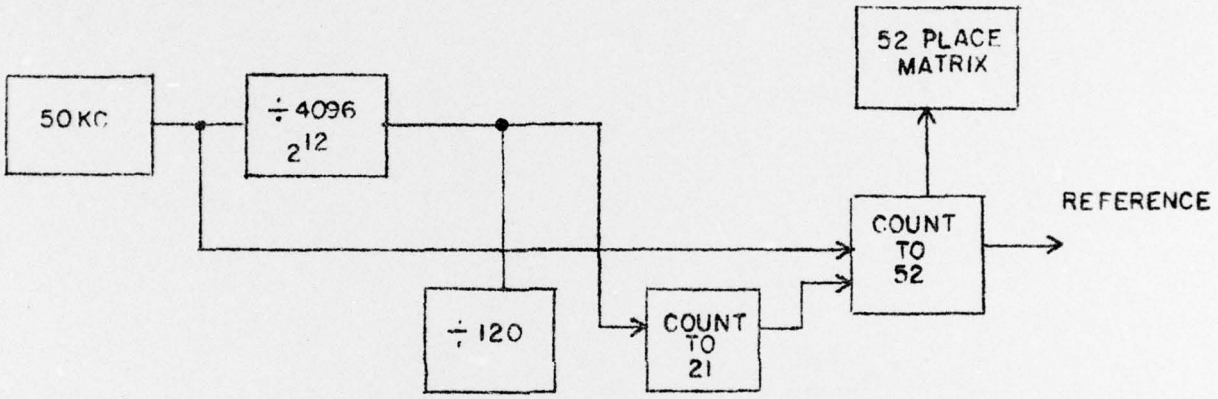
The output of the eight flip flops would be further gated through the arithmetic structure to the core memory and reset. This could complete the initial phase of processing of data to present it to the memory.

The matrix switching pulses to the analyzer integration capacitors will be provided every 1/12 second, or the time interval required for the beam to scan three degrees. The programming sequence will be 1092, 20 μ second pulses occurring every 1/12 second.

Programming

Only elementary programming instrumentation will be considered initially. It is conceivable to scan the 1092 integrators and read their outputs during the non-writing intervals. However, this type of programming will enhance the display, but not add to the data or improve the processing. Therefore, this phase will be carried out at a later time.

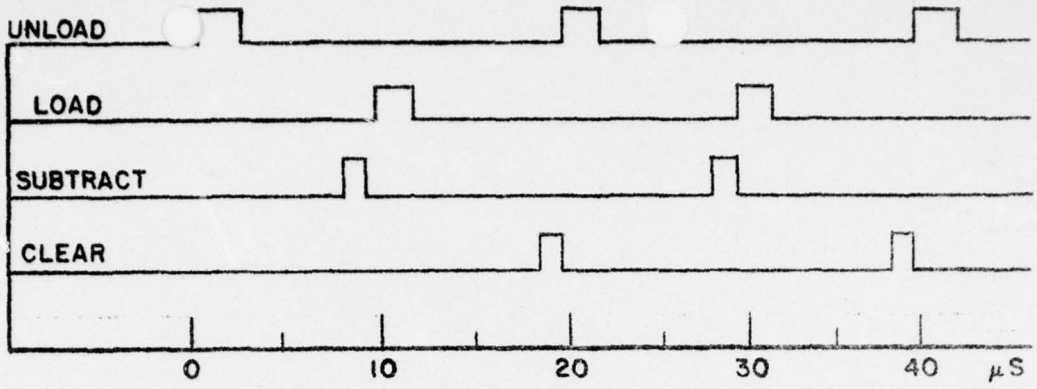
The basic clock period source will be 50 kc (nominal) square wave. This will slave, if necessary, to the synchronous scan. A block diagram of the basic divider chain is shown:



Required are 21 groups of 52, 20 microsecond spaced pulses. This will allow a maximum of 52 analyzer channels, of which 50 are planned to be used. The 21 groups will be used to represent the data in each of 21, 3 degree beams. The scan rate is 36 degrees per second. The 21 beamwidths should be filled in 1.75 seconds.

The 50 kc frequency control signal will be divided by 2^{12} or 4096 to 12 cps. The 50 kc is a nominal value, for it actually is very slightly lower, making the pulse periods slightly greater than 20 microseconds. The 12 cps pulses are counted and passed up to 21 in number. This action is cycled every 10 seconds by a 120 to 1 divider. Each time a 12 cycle pulse is passed, it gates a group of 52, 20 μs pulses to the core memory.

The output pulses represent the reference or unload pulses to the core memory. The other pulses operating the unit shall be derived from them. The time relationships of the other pulses to the reference or unload pulse appear as follows:



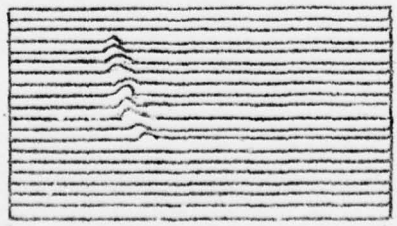
The above three pulses will be derived from the unload pulse by means of delay multivibrators.

The scanning will have to be precisely regulated in speed to achieve the maximum degree of congruence of the successive overlying frames of data. For this reason, it may be necessary eventually to slave a frequency control loop between the scanning transducer and the 50 kc oscillator. However, this is to be regarded as a second phase investigation effort.

Display

Optimum use of the tactical display features will not be incorporated into the initial instrumentation. There are several reasons for not making more effective use of the capability at this time, but the primary one is of complication of the instrumentation. It is not reasonable with the effort planned to utilize the full capability. Furthermore, the effect may not be realistic in a general case. By this, it is meant that only a 63 degree sector will be processed. The principle enhancement of the display could be made principally by utilizing the "dead" time between repetitions of the scanning of this 63 degree sector.

The eight output leads of the core memory are weighted in a binary manner. A parallel binary voltage-to-analogue converter can be instrumented. For the required accuracy, 1 part in 256, a vacuum tube cathode follower summation circuit can be used. This output, now in serial form, can be displayed in several ways. The most expeditious will be to use the memotron oscilloscope and establish 21 traces in a "B" scan manner. Instead of intensity modulation, amplitude or A scan data can be interposed on each of the traces producing s display appearing as follows:



It is also planned to make comparisons of data processed by the integrators using conventional PPI displays.

It is also possible at the digital-to-analogue converter to introduce rather simply a fixed number so that only values greater than it will be passed to the display. This might be done in a later phase of investigation.